

Samsung 3bit 3D V-NAND technology

Yield more capacity, performance and power efficiency



Stay abreast of increasing data demands with Samsung's innovative vertical architecture

Introduction

There continues to be an explosive growth in data traffic worldwide, pushing NAND flash memory to its limits. Current 2D planar NAND technology has inherent limitations, preventing capacity expansion that would result in critical degradation of performance and reliability. Since 2D planar NAND cannot effectively scale capacity to meet increasing data demand, new solutions must be found.

Samsung offers an innovative solution to satisfy rising data demands with its cutting-edge, 3bit 3D vertical-NAND (V-NAND) flash technology. By stacking memory cells vertically in a three-dimensional structure, new potential for 3D memory capacities are created, eliminating performance and reliability issues from capacity limitations. Whether end consumers or data centers, everyone can expect smooth, reliable performance at lower costs for today's demanding, data-centric world.

Traditional 2D planar NAND technology

A typical NAND flash chip is composed of memory cells on a plane that enables memory write capabilities. The more cells there are, the greater the memory capacity. Manufacturers strive to fit more cells in less space and in merely 15 years cell size has gone from 120 nm to 19 nm with 100 times more capacity, reaching today's cell size of 1x nm.

Cell-to-cell interference

Continually shrinking the cells creates technical challenges that arise from an electrical charge in a cell flowing into an adjacent cell creating cell-to-cell interference. This cell-to-cell interference unfortunately leads to data corruption. And when a cell size goes below 20 nm, the chance for interference drastically increases, inevitably making the cell unreliable.

Prohibitive patterning

Patterning is a photolithography process that uses light to transfer a geometric pattern from a mask to a photoresist on the substrate of the chip to create a circuit. With a 1x nm sized cell, light is unable to penetrate the mask. Effective, shorter wavelength light equipment is an alternative, but is cost prohibitive.

Samsung 3bit 3D V-NAND memory technology

Samsung's revolutionary 3bit 3D V-NAND technology features a unique design that stacks 32 layers of 3bit cells on top of one another instead of trying to decrease the cells' length and width to fit into today's ever-shrinking form factors. Using this new 3D V-NAND architecture creates two times the density of a traditional 2D planar NAND in a smaller footprint.

Compared to Samsung's 2-bit 32-layer V-NAND technology, the 3bit V-NAND flash has crossed the threshold of costs in dollars per gigabit by being able to store 3 bits per cell over 2 bits per cell. This disruptive density 3bit technology brings costs down, yet still offers better endurance for consumer and enterprise applications. By delivering cost, value and density, it enables Samsung to increase the level of support for next-generation interfaces, advancing the SSD market.

Disruptive Density



This innovative design eliminates pattern limitations while achieving a much larger scalable capacity to satisfy present and future data demands. 3D V-NAND's unique design is achieved by disruptive innovation of structure, material and integration.

Realize increased capacity with a higher-density cell structure

Material innovation

Using Charge Trap Flash (CTF) technology, Samsung's 3D V-NAND flash memory boasts a cell-to-cell interference-free structure. CTF technology uses a non-conductive layer of silicon nitride (SiN), which temporarily traps electrical charges to maintain cell integrity. This non-conductive layer is modified into a three-dimensional form to wrap around the control gate of the cell, acting as an insulator that holds charges, to prevent data corruption caused by cell-to-cell interference.

Structural innovation

To create the vertical integration of 3D V-NAND cell layers, Channel Hole Technology is used. This technology enables cells to connect vertically with one another through a cylindrical channel that runs through each column of stacked cells. The 32-layer stacks of cells are connected to over 2 billion channel holes that are etched from the top layer of the NAND to the bottom layer. Looking from a top-down view, all the holes can be seen on a 128 Gb NAND chip that is the size of a fingernail.

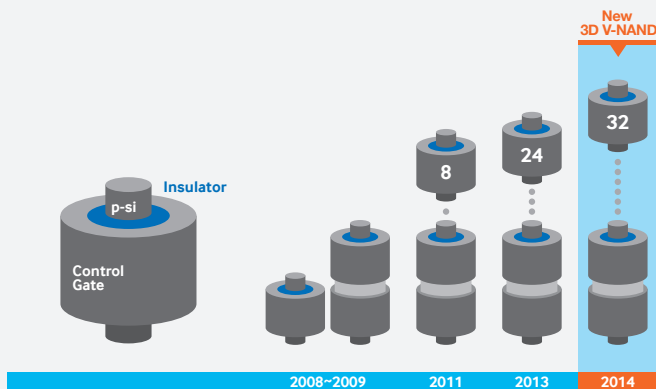
Integration innovation

The cylindrical channels enable seamless integration of the vertical layers of cells.

This 3D V-NAND technology improves memory in several essential areas:

- Capacity for high-quality data
- Speed for faster performance
- Endurance for more traffic
- Efficiency for resource conservation

Integration Innovation

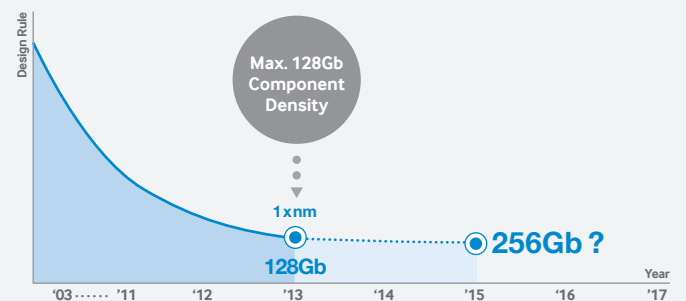


More layers equals more capacity

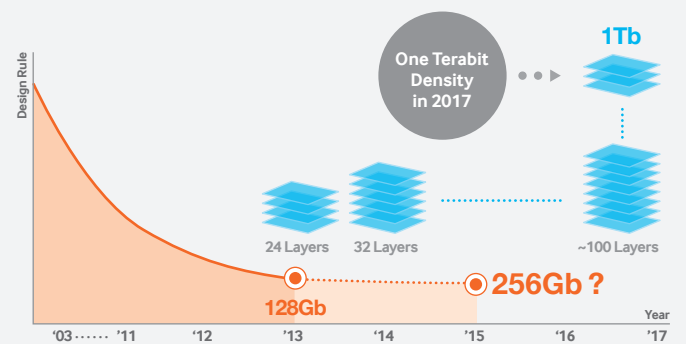
NAND flash capacity is determined by the number of memory cells that can fit in a NAND chip, hence, the importance of shrinking cells to fit more into less space. Samsung 3D V-NAND technology offers significantly more capacity. By layering cells vertically in three-dimensional stacks, Samsung 3D V-NAND technology provides much greater cell density. As a result, heavy workload users and data centers can store and handle data over a longer period of time with greatly improved capacity. The 3bit 3D V-NAND technology enables cost scaling, lowering costs while maximizing storage capacity.

Even with cell shrinkage beyond 1x nm, the 2D planar NAND design limits the maximum component density to 128 Gb. However, the innovative 3D V-NAND design enables up to 100 layers of cells to be stacked with the potential to scale density up to 1 Terabyte (TB) by 2017. This is a major breakthrough in capacity. For comparison, the 2D planar NAND density ceiling can only reach the minimum density of 3D V-NAND.

2D Planar NAND Capacity Limitation



3D V-NAND Capacity Breakthrough



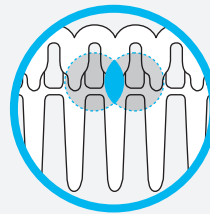
Double data write speeds compared with 2D NAND with unique algorithms

Innovative algorithms equals faster performance

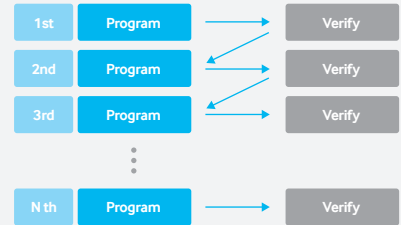
NAND flash memory speeds are based on the complexity of the program algorithms that write the data. Traditional 2D planar NAND flash requires the creation of very precise sets of complex program algorithms to prevent data corruption caused by cell-to-cell interference. Running these highly complex algorithms requires additional time for data to be written, resulting in slower speeds.

However, because Samsung 3bit 3D V-NAND technology is virtually immune to cell-to-cell interference, it can write data significantly faster. By using distinctive program algorithms, Samsung's 3bit 3D V-NAND flash memory can write up to two times faster than traditional 3bit 2D planar NAND flash memory. The result is significantly improved performance, which is ideal for data center workloads.

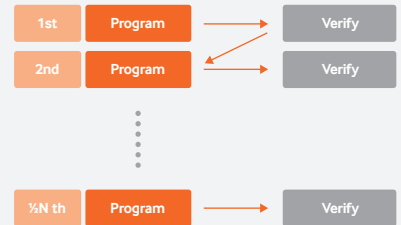
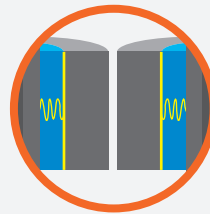
2D Planar NAND



<20nm



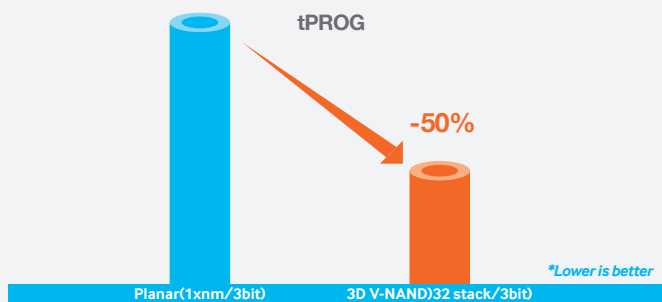
3D V-NAND



Innovative Algorithm

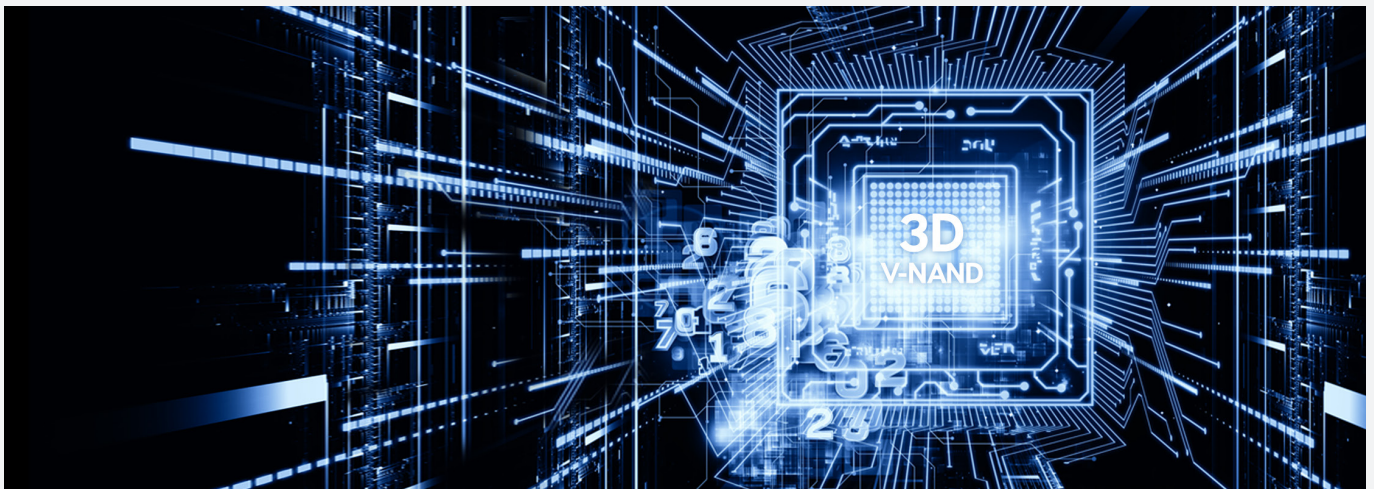
Approximately 2X Faster

V-NAND Speed



Program Algorithm

The virtual immunity to cell-to-cell interference in the 3D V-NAND enables it to deliver unsurpassed write speeds - up to twice that of 2D planar NAND flash memory.



Experience unparalleled reliability and greater power efficiency

Less overlap and less errors means higher endurance and reliability

Electric fields produced by cell material and the structure affect the endurance of a NAND flash memory chip. The higher the electric field, the more stress is placed on a chip and, in turn, the lower its endurance. However, the unique materials and structure of 3D V-NAND flash memory decreases its electric field, thereby improving its endurance and enabling more data traffic over a longer duration.

The conductors in 2D planar NAND memory cells, along with the planar structure, allow electrical charges to pass through, rendering a relatively higher electric field. This higher electric field, in turn, lowers its endurance and reduces its lifespan. In contrast, 3D V-NAND cells are slightly larger and employ CTF-based insulators, enabling it to hold more electrical charges, making it more resistant to wear and reducing the risk of cell-to-cell interference. As a result, the 3D V-NAND experiences less stress and delivers more endurance - up to twice that of 2D planar NAND.

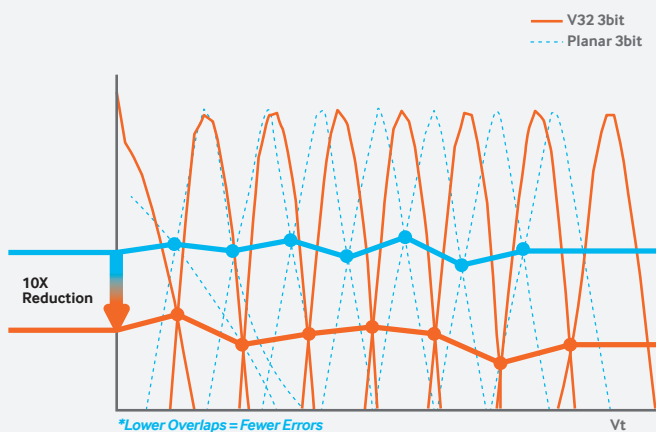
Samsung 3bit 3D V-NAND technology boasts more error resistance than previous V-NAND chips and 3bit 2D planar NAND. Its superb voltage distribution reduces overlaps, which directly improves the bit error rate with a reduction rate up to ten times that of 3bit planar NAND memory.

Less programming steps equals lower power consumption

To lower the effects of cell-to-cell interference, traditional 2D planar NAND flash must perform a large number of programming steps, which increases power consumption. Because Samsung's 3D V-NAND technology has eliminated the issue of interference, its programming steps are greatly reduced. As a result, power consumption is substantially lowered by up to 45 percent compared to 2D planar NAND memory.

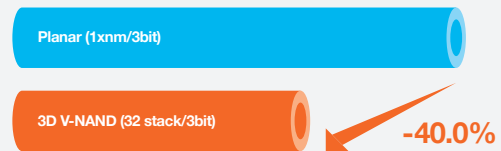
Samsung's 3bit 3D V-NAND memory cells boast greater endurance and lower power consumption than 3bit 2D planar NAND memory.

V-NAND Reliability



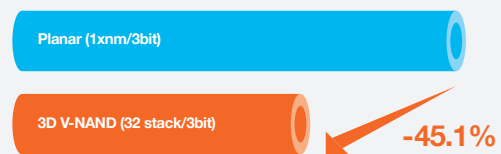
Voltage Distribution Comparison

V-NAND Speed



Charge Consumption @ Program

*Lower is better



Charge Consumption @ Read

*Lower is better

Improve capacity, performance, endurance and power efficiency

Conclusion

Samsung 3bit 3D V-NAND flash technology overcomes the capacity limitations of traditional 2D planar NAND technology with its revolutionary vertical, three-dimensional design. This innovative 3D vertical architecture insulates individual cells from interference and increases density to eliminate patterning restrictions.

In addition, the innovations that 3D V-NAND flash provide enable higher cell density for greater capacity, simplified programming for enhanced speed and power efficiency, and robust materials for greater endurance over the lifespan of the flash memory. Samsung 3D V-NAND flash memory is the smart choice for fulfilling the ever-increasing demands of today's - and tomorrow's - data centers.

Choose flash memory designed by a pioneer in 3D V-NAND technology

Samsung has gained a wealth of knowledge and expertise as a global leader in memory innovations, which spans more than two decades. Over those years, Samsung boasts a number of market firsts, including the first SSD, the first 2-bit MLC SSD, the first 3bit SSD and the first PCIe PC SSD.

In particular, Samsung is a major innovator in V-NAND memory technology and the first company to mass-produce 3D V-NAND-equipped SSDs. And now Samsung is the first to develop the 32-stack 3bit

V-NAND. No wonder so many data centers are entrusting Samsung flash memory to manage their valuable data.

Samsung has been a global leader in designing and manufacturing cutting-edge memory technology spanning more than two decades.

Legal and additional information

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For more information

For more information about Samsung 3bit 3D V-NAND flash memory, visit

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